Adaptive Voltage Controlled Nanoelectronic Addressing for Yield, Accuracy and Resolution

Bao Liu
Electrical and Computer Engineering Department
The University of Texas at San Antonio
San Antonio, TX 78249-0669
Email: bliu@utsa.edu

ABSTRACT

An outstanding challenge for realizing nanoelectronic systems is nano-interface design, i.e., how to precisely access a nanoscale wire in an array for communication between a nanoscale system and the outside world. Existing nanoelectronic addressing methods are based on implementation of binary decoders, which requires unrealistic precise layout design in nanotechnology. In this paper, I propose voltage controlled nanoelectronic addressing, which differentiates each nanoscale wire by their electrical parameters, e.g., voltages, instead of required unique physical structures. As a result, voltage controlled nanoelectronic addressing achieves significant yield improvement, which enables aggressive scaling of nano-interface with the rest of a nanoscale system. A novel nanoelectronic addressing circuit includes two address lines which form resistive voltage dividers, and provide gate voltages for two rows of transistors which gate the nanoscale data lines. For two proposed nanoelectronic addressing metrics: resolution and accuracy, the proposed circuit achieves single data line resolution by applying high voltage drops to the address lines if not high subthreshold slope transistors, while an adaptive addressing method achieves addressing accuracy only depending on the uniformity of the address lines, and external time domain variations. SPICE simulation based on compact CNFET models demonstrates the effectiveness of voltage controlled nanoelectronic addressing.

I. INTRODUCTION

While silicon based technology is rapidly approach its end [8], recent development in nanotechnology has led to successful fabrication of a number of nanometer scale devices, e.g., resonant-tunnel diodes (RTDs) [18], molecular bistable devices [15], and carbon nanotube transistors (CNFETs) [17]. This has provided great opportunity for VLSI circuits to continue scaling in a post-silicon-based-technology era based on these nanometer scale devices. Consequently, nanoelectronic circuit design and system integration techniques have been under active research.

Traditional top-down lithography based VLSI manufacturing processes cannot achieve satisfiable resolution as minimum layout feature sizes become smaller than lithography light wavelengths. Alternatively, nanoscale device integration is anticipated to be based on bottom-up self-assembly manufacturing technologies, for example, molecular beam epitaxy (MBE), which provide regular (such as crossbar) structures [14]. Nanoelectronic circuits are also expected to be subject to prevalent defects and significant parametric variations, due to manufacturing process limitation, aggressive design, and ultimately the uncertainty principle of quantum physics, which make them inevitable at nanometer scale. As a result, nanoelectronic design must rely on configuration of regular structures to achieve not only functionality but also reliability.

Among various nanoscale devices, carbon nanotubes and carbon nanotube transistors are the most promising candidates for the building blocks of next generation VLSI systems. Carbon nanotubes form excellent nanometer scale interconnects due to their extraordinary electrical current carry capability, thermal conductance, and mechanical stress [11, 19]. MOSFET-like carbon nanotube based field effect transistors (MOSFET-like CNFETs) are unipolar devices behaving the same as the existing MOSFETs, making them ideal to build nanoelectronic circuits in the same style as the current CMOS circuits. Alternatively, band-to-band tunneling carbon nanotube field effect transistors (T-CNFETs) have the potential to achieve ultra high on-off current ratio and subthreshold slope, making them ideal for next generation of ultra low power and
high performance circuits.

Consequently, carbon nanotube crossbar structure (Fig. 1) is one of the most prominent candidates for nanoelectronic architecture [14], which is expected to form the basis of nanoscale memories [4, 21], and provide a reconfigurable computing platform for nanoelectronic systems of manufacturability and reliability [9]. Researchers at UIUC have recently achieved significant progress towards such carbon nanotube crossbar structures with the fabrication of dense perfectly aligned carbon nanotube arrays [7].

However, an outstanding challenge for realizing such nano-electronic systems is how to precisely address an individual nanoscale wire (e.g., carbon nanotube) in an array. Designing a nanoelectronic addressing circuit is a challenging task, because (1) the nanoscale layout cannot be manufactured precisely unless it is of a regular structure, and (2) the nanoelectronic addressing circuit cannot be based on reconfigurability since it provides reconfigurability to the rest of the nano-electronic system. Existing nano-electronically addressing circuits require precise layout control such as lithography [6], doping [2], or etching [13], which is highly unlikely to achieve at the nanometer scale due to the presence of prevalent defects and significant process variations. They also exhibit certain levels of randomness [2, 6, 20], which brings unaddressable or undifferentiated nanoscale wires, and requires testing schemes which associate nanoscale wires with addresses.

The contributions of this paper include: (1) a voltage controlled nano-electronic circuit of simple layout design which achieves improved yield and enables aggressive nano-interface scaling in concurrence with the rest of a nanoscale system, (2) evaluation of the proposed voltage controlled nano-electronic circuit, with two newly proposed quantitative metrics for nano-electronic addressing: resolution and accuracy, and (3) methods to achieve nano-electronic addressing resolution and an adaptive addressing method which achieves nano-electronic addressing accuracy depending only on address line uniformity and external time domain variations.

The rest of this paper is organized as follows. Section II gives a brief review of the existing binary decoder based nano-electronic addressing mechanisms. Section III presents the proposed voltage controlled nano-electronic addressing circuit. Section IV gives its evaluation, two proposed nano-electronic addressing metrics: resolution and accuracy, and SPICE simulation result. Section V presents techniques for nano-electronic addressing resolution, and an adaptive nano-electronic addressing method for nano-electronic addressing accuracy. Section VI concludes this paper.

II. BACKGROUND

A nano-electronic addressing circuit provides an interface for communication between a nanoscale system and the outside world. It can be applied for address decoders and bitline multiplexers in a nanoscale memory, as well as configuration, testing, and data I/O in a nano-electronic circuit. Traditionally it consists of a crossbar of orthogonal microscale wires and nanoscale wires (e.g., Fig. 2). Electrical signals (address signals) coming from the microscale wires (address lines) supposedly select one of the nanoscale wires (data lines) to be conductive (for data I/O). The existing nano-electronic addressing circuits are binary decoders, i.e., every nanoscale wire is selected by a (supposedly unique) binary address. This requires that each nanoscale wire needs to have a unique gate configuration. However, such precise layout design is unlikely to achieve at a sublithographic nanometer scale, where a top-down lithography based manufacturing process cannot achieve substantial yield, while a bottom-up self-assembled manufacturing process simply provides only regular structures.

Existing nano-electronic addressing mechanisms are in four categories.

1. Randomized contact decoder [20] includes gold particles which are deposited at random as contacts between nanoscale and microscale wires. Testing and feedback provide a one-to-one mapping between a nanoscale wire and an address.

2. Undifferentiated nanoscale wires are addressed by microscale wires with (e.g., lithography defined) different gate configurations (which requires nanoscale wire spacing in the same order of lithography resolution) [6] (Fig. 2).

3. Alternatively, different gate configurations are realized in the nanoscale wires, by growing lightly-doped and heavily-doped carbon nanotubes of different length alternatively, while the microscale wires are undifferentiated. A microscale wire crossing a lightly-doped nanotube segment forms a gate, while a heavily-doped nanotube segment is always conductive for all possible signals in the microscale wire. In such a case, precise control of the lengths of the lightly- and heavily-doped nanotube segments would be critical [2, 5].

4. In radial addressing, multi-walled carbon nanotubes are grown with lightly- and heavily-doped shells, wherein an etching process removes the heavily-doped outer shells at precise locations, and defines the gate configurations at each crossing of nanoscale and microscale wires [13].

Process variations are prevalent and significant at nanometer scale due to manufacturing limitation, aggressive design,
and ultimately the uncertainty principle of quantum physics which makes them inevitable. As a result, these existing nano-electronic addressing structures can achieve only very limited yield, e.g., there is certain probability that two nanoscale wires have identical or similar gate configuration due to process variation. Furthermore, nanoscale wires are mostly partially selected, e.g., they may not achieve the ideal conductivity upon selection, due to process variations such as misalignment, dopant variation, etc.

III. DESIGN OF VOLTAGE CONTROLLED NANO-ELECTRONIC ADDRESSING CIRCUIT

A. Principle

The proposed voltage controlled nanoscale wire addressing circuit (Fig. 3) is constructed by running two address lines (of either microscale or nanoscale wires) orthogonal on top of the data lines (of nanoscale wires in an array which are to be addressed), and forming field effect transistors at each crossing of an address line and a data line. The address lines are voltage dividers, they are driven by external voltage sources \(V_{l1}\) and \(V_{r1}\) for address line 1, \(V_{l2}\) and \(V_{r2}\) for address line 2) and provide gate voltages to the transistors, which gate the data lines. Given an array of decreasing/increasing gate voltages at the first(second) address line respectively (e.g., \(V_{l1} > V_{r1}, V_{l2} < V_{r2}\)), the transistors on the right(left) side at the first(second) address line are turned off or of negligible current, while the data line of peak current is in the middle of the array. Adjusting the external voltages selects a specific data line of peak current, while the other data lines are of negligible currents. In this way, this addressing circuit functions as a multiplexer, allowing a single data line to connect to the microscale wire for data I/O. The data lines can be either wordlines or bitlines of a memory, configuration data I/Os, or primary inputs/outputs of a nanoscale circuit.

B. Manufacture

The field effect transistors at the crossings of address lines and data lines can be formed by doping the data line into the source and the drain regions, while the address line provides the gate of the transistor, with a thin layer of dielectric sandwiched between the gate and the transistor channel. Such field effect transistors have been manufactured based on either nanowires or carbon nanotubes [4, 12, 17].

Carbon nanotubes are either metallic or semiconductive based on their chirality [11], which is hardly controllable in current technology. As a result, about one third of fabricated carbon nanotubes are metallic. These metallic carbon nanotubes can be removed by either electrical breakdown [1] or selective etching [22]. The remaining semiconductive carbon nanotubes need to be doped to form the transistors in the nanoelectronic addressing circuit, and to form the active regions of transistors in the (reconfigurable) nanoelectronic circuit.

IV. EVALUATION OF VOLTAGE CONTROLLED NANO-ELECTRONIC ADDRESSING CIRCUITS

A. Yield

The proposed voltage controlled nanoelectronic addressing circuit implies significant yield improvement compared with the existing binary decoder based nanoelectronic addressing circuits.

1. The existing binary decoder based nanoelectronic addressing circuits require every nanoscale wire to have a unique physical structure to differentiate itself, which is highly unlikely to achieve in a nanoscale manufacturing process - lithography cannot achieve nanoscale resolution, while bottom-up self-assembly based nanoscale manufacturing processes provide only regular structures. Even at microscale, such a structure is subject to prevalent catastrophic defects and significant parametric variations, and results in low yield.

2. On the contrary, the proposed circuit consists of only an array of identical components. Every nanoscale wire has a uniform physical structure and is differentiated only by their electrical parameters, e.g., the node voltages. This scheme avoids complex layout design, significantly improves yield, and enables aggressive scaling of the addressing circuit with the rest of the nanoelectronic system.

B. Process Variation Effects

A variety of process variations are expected to be prevalent and significant in nanoelectronic systems. Their effects on the addressing circuit are as follow.

1. Global address line resistance variations, including width, height, and resistivity variations which are identical for every segment of the address lines, have no effect on the voltage divider hence the addressing scheme.

2. Address line misalignment has no effect on the conductances of the data lines.
3. Global data line misalignment (i.e., shifting of all data lines), as well as variations of external voltage sources and the external (wire and contact) resistance between the resistive voltage divider and the external voltage sources, lead to potential addressing inaccuracy (Definition 1).\(^1\)

4. Individual data line misalignment could decrease the difference between the gate voltages of two adjacent transistors, leading to higher resolution (Definition 2) requirement to distinguish the two adjacent data lines.

5. Process variations of the transistors, including width, length, dopant concentration, and oxide thickness variations, lead to transistor conductivity uncertainty and require higher addressing resolution (Definition 2). The addressing scheme needs to provide a conductivity difference for two adjacent data lines which is larger than the process variation induced data line conductivity uncertainty.

C. Metrics

Since no quantitative metrics has been proposed for nanoelectronic addressing to the best of the author’s knowledge, I propose two quantitative metrics for nanoelectronic addressing as follow.

**Definition 1** Addressing resolution is the minimum current ratio between the data line of peak current and an adjacent data line.

\[
R_A = \frac{I_1}{I_2}
\]

where \(I_1\) is the peak current, \(I_2\) is the larger current of the two data lines which are adjacent to the data line of peak current.

**Definition 2** Addressing inaccuracy is the offset between the data line of peak current and the data line of intended address.

\[
A_A = A_1 - A_0
\]

where \(A_1\) is the address of the data line of peak current, \(A_0\) is the intended address.

D. Simulation

We now look at SPICE simulation based on the Stanford CNFET compact model [3] for the proposed voltage controlled nanoelectronic addressing circuit (Fig. 3) implemented with carbon nanotubes (CNTs) and N-type MOSFET-like carbon nanotube field effect transistors (CNFETs). The CNFETs are of 6.4nm gate width and 32nm channel length, as is given by the Stanford CNFET compact model. The two CNFETs in each nanotube are given a voltage drop of \(V_{dd} = 1V\) across their active regions (larger voltage drops across the CNFET active regions do not lead to much improvement in addressing resolution since the CNFETs are in saturation, while smaller voltage drops lead to degraded addressing resolution). The external address voltages are \(V_{g1} = V_{g2} = 1V\), \(V_{g1} = V_{g2} = 0\) (which provides a zoomed-in picture centered around the nanoscale data line of peak current for larger voltage drops along the address lines). Fig. 4 shows carbon nanotube current as a function of the gate voltage of the transistor at the first address line. The same curve can also be taken as the current profile of the nanoscale data lines in an array addressed by the proposed circuit. The nanotubes carry a significant current only with specific gate voltages, e.g., reaching \(I_{out} = 5.064mA\) at gate voltage \(V_{g1} = 0.495V\). This allows us to adjust the gate voltage via the external address voltages, and address a specific carbon nanotube in the array.

V. ADAPTIVE VOLTAGE CONTROLLED NANOELECTRONIC ADDRESSING

A. Resolution

To achieve single data line addressing resolution, two adjacent nanoscale data lines must carry significantly different currents. This can be achieved by the following two techniques.

1. Increase CNFET inverse subthreshold slope.

The I-V slope in Fig. 4 is limited by the inverse subthreshold slope of the transistors in the circuit. The inverse subthreshold slope \(S\) is the minimum gate voltage variation needed to bring a \(10\times\) source-drain current increase, which is \(2.3\frac{kT}{q} \approx 60mV/\text{decade}\) at 300K for MOSFETs and MOSFET-like CNFETs [17]. Research on alternative devices, e.g., band-to-band tunneling CNFETs, can potentially lead to larger inverse subthreshold slopes.

2. Increase the external voltage drop across the address lines.

Alternatively, single data line addressing resolution is achievable by applying well separated gate voltages to the adjacent data lines. This implies high voltage drop across the address lines. High voltages bring reliability issues such as electromigration and gate dioxide breakdown. Fortunately, carbon nanotubes are highly resistive to electromigration due to its high resistivity and excellent current carrying capability, while we have known materials which resist up to 200kV high voltage [10].

---

\(^1\)Adaptive nanoelectronic addressing (e.g., Method 1) cancels these process variation effects on nanoelectronic addressing accuracy.
B. Accuracy

After achieving single nanoscale data line resolution, addressing accuracy is achievable by an adaptive procedure (Method 1). We first exam the external voltage offset needed for a data address offset as follows.

Suppose (Fig. 5) for the k-th address line (k = 1 or 2), the external voltages \( V_{lk} \) and \( V_{rk} \) address the i-th data line \( D_i \). The resistances on the left side and the right side of the data line \( D_i \) are \( R_l \) and \( R_r \), respectively. We have

\[
\frac{R_l}{\sum R} V_{lk} + \frac{R_r}{\sum R} V_{rk} = V_{on}
\]

(3)

where \( \sum R = R_l + R_r \) is the total resistance of an address line, \( V_{on} \) is the voltage needed to address a data line of peak current. Shifting the external voltages to \( V_{lk} + \Delta V \) and \( V_{rk} + \Delta V \) addresses another data line \( D_j \). The resistances on both sides of the data line \( D_j \) are \( R_l + \Delta R \) and \( R_r - \Delta R \), respectively. We have

\[
\frac{R_r - \Delta R}{\sum R} (V_{lk} + \Delta V) + \frac{R_l + \Delta R}{\sum R} (V_{rk} + \Delta V) = V_{on}
\]

(4)

As a result,

\[
\Delta V = \frac{\Delta R}{\sum R} (V_{lk} - V_{rk})
\]

(5)

Observation 1 The external voltage offset \( \Delta V \) is proportional to the resistance offset \( \Delta R \) of the addressed data lines, and is proportional to the physical offset \( \Delta L \) of the addressed data lines, given the resistive voltage dividers are uniform (e.g., the data lines are equally spaced and the address lines have uniform resistivity).

Based on Observation 1, Method 1 gives an adaptive nanoelectronic addressing method, which finds the external voltage shifts needed to address the left most and the right most data lines first. Any other external voltage shift needed to address a specific data line is then computed based on a linear interpolation. To address the left most or the right most data line, we apply a gradually increasing/decreasing external voltage offset \( \Delta V \) at one of the address lines, keep all the transistors at the other address line on, and measure the conductance between two microscale wires which connect to the data lines at their opposite ends. The maximum and the minimum \( \Delta V \)'s (e.g., \( \Delta V_{\text{min}} \) and \( \Delta V_{\text{max}} \)) with non-zero conductances between the two microscale wires address the left most and the right most data lines, respectively.

Method 1: Adaptive Voltage Controlled Nano Addressing

Given: \( n \) nanoscale data lines, address \( i \)

Address: \( i \)-th data line

1. Achieve single line resolution, e.g., by increasing \( |V_{lk} - V_{rk}| \)
2. Set \( V_{l2} \) and \( V_{r2} \) to turn on all the transistors at address line 2
3. Shift \( V_{l1} \) and \( V_{r1} \) by \( \Delta V_{\text{min1}} \) to address the left most data line
4. Shift \( V_{l1} \) and \( V_{r1} \) by \( \Delta V_{\text{max1}} \) to address the right most data line
5. Set \( V_{l1} \) and \( V_{r1} \) to turn on all the transistors at address line 1
6. Shift \( V_{l2} \) and \( V_{r2} \) by \( \Delta V_{\text{min2}} \) to address the left most data line
7. Shift \( V_{l2} \) and \( V_{r2} \) by \( \Delta V_{\text{max2}} \) to address the right most data line
8. To address the i-th data line (from the left)
   - Shift \( V_{l1} \) and \( V_{r1} \) by \( \frac{\Delta V_{\text{min1}}}{i} + \frac{\Delta V_{\text{max1}}}{n-1} \)
9. Shift \( V_{l2} \) and \( V_{r2} \) by \( \frac{\Delta V_{\text{min2}}}{i} + \frac{\Delta V_{\text{max2}}}{n-1} \)

VI. Conclusion

Voltage controlled nanoelectronic addressing achieves significant yield improvement and enables aggressive scaling of nano-interface with the rest of the nanoscale system, by differentiating each nanoscale wire by their electrical parameters, e.g., voltages, instead of required unique physical structures. Single data line resolution is achievable by applying high voltage drops to the address lines if not high subthreshold slope transistors, while addressing difficulty given by an adaptive addressing method depends only on the uniformity of the address lines, and external time domain variations. SPICE simulation based on compact CNFET models proves the effectiveness of the proposed voltage controlled nanoelectronic addressing scheme.

REFERENCES


